CLAIMS

What is claimed is:

1. A switching fabric comprising

N/D P×M input nodes having output ports,

M/D N×Q output nodes having input ports, and

an interstage exchange interconnecting each one of the input nodes to each one of the output nodes with D lines, each of the lines interconnecting a distinct one of the output ports and a distinct one of the input ports, where $D > 1$, and D is a common factor of M and N.

2. The switching fabric as recited in claim 1 wherein $M = 2^{n-r}$, $N = 2^r$, and $D = 2^d$, with $1<r<n$ and $1\leq d<\min(r, n-r)$.

3. The switching fabric as recited in claim 2 wherein the interstage exchange is a bit-permuting exchange induced by a permutation π on integers from 1 to n–d such that the images of the numbers r–d+1, r–d+2, …, n–d cover the numbers 1, 2, …, n–r–d, or equivalently, the images of the numbers 1, 2, …, r–d are covered by the numbers n–r–d+1, n–r–d+2, …, n–d.

4. The switching fabric as recited in claim 3 wherein $P = 2^{n-r}$ and $Q = 2^r$.

5. The switching fabric as recited in claim 4 wherein each one of the input nodes is constructed from a k_1-stage $2^{n-r}\times 2^{n-r}$ bit-permuting network of cells and each one of the output nodes is constructed a k_2-stage $2^r\times 2^r$ bit-permuting network of cells such that the switching fabric is a k-stage $2^{n-d}\times 2^{n-d}$ bit-permuting network of cells with $k=k_1+k_2$.

6. The switching fabric as recited in claim 5 wherein the trace and the guide of the k-stage bit-permuting network are respectively a k-term sequence containing the numbers from 1 to n.

7. The switching fabric as recited in claim 6 wherein each of the $D= 2^d$ lines is replaced by a bundle of b lines, b>1, and each of the cells is dilated proportionately.

8. A switching network constructed from recursive 2-stage construction, one of the recursive steps constructing a modified 2-stage interconnection network, the modified 2-stage interconnection network comprising

N/D P×M input nodes having output ports,

M/D NxQ output nodes having input ports, and

an interstage exchange interconnecting each one of the input nodes to each one of the output nodes with D lines, each of the lines interconnecting a distinct one of the output ports and a distinct one of the input ports, where $D > 1$, and D is a common factor of M and N.

9. The switching network as recited in claim 8 wherein $M = 2^{n-r}$, $N = 2^r$, and $D = 2^d$, with $1<r<n$ and $1\leq d<\min(r, n-r)$.

10. The switching network as recited in claim 9 wherein the interstage exchange is a bit-permuting exchange induced by a permutation π on integers from 1 to n–d such that the images of the numbers r–d+1, r–d+2, …, n–d cover the numbers 1, 2, …, n–r–d, or equivalently, the images of the numbers 1, 2, …, r–d are covered by the numbers n–r–d+1, n–r–d+2, …, n–d.

11. The switching network as recited in claim 10 wherein $P = 2^{n-r}$ and $Q = 2^r$.

12. The switching network as recited in claim 11 wherein each one of the input nodes is constructed from a k_1-stage $2^{n-r}\times 2^{n-r}$ bit-permuting network of cells and each one of the output nodes is constructed from a k_2-stage $2^r\times 2^r$ bit-permuting network of cells such that the modified 2-stage interconnection network is a k-stage $2^{n-d}\times 2^{n-d}$ bit-permuting network of cells with $k=k_1+k_2$.

13. The switching network as recited in claim 12 wherein the trace and the guide of the k-stage $2^{n-d}\times 2^{n-d}$ bit-permuting network are respectively a k-term sequence containing the numbers from 1 to n.

14. The switching fabric as recited in claim 13 wherein each of the $D=2^d$ lines is replaced by a bundle of b lines, b>1, and each of the cells is dilated proportionately.

15. A switch based upon a plurality of opto-electrical-physical implementation levels comprising

N/D first switching elements, each having P input ports and M output ports and having a configuration based on a first one of the implementation levels,

M/D second switching elements, each having N input ports and Q output ports and having a configuration based on a second one of the implementation levels, and

an interface circuit, which is compatible with both the first implementation level and the second implementation level, interconnecting each of the first switching elements to each of the second switching elements with D lines, each line interconnecting a distinct one of the output ports of the first switching elements and a distinct one of the input ports of the second switching elements, where $D > 1$, and D is a common factor of M and N.

16. The switch as recited in claim 15 wherein the interface circuit has MN/D input ports to cooperatively interconnect with the MN/D outputs of the N/D first switching elements, MN/D output ports to cooperatively interconnect with the MN/D inputs of the M/D second switching elements, and interconnections between the MN/D input ports of the interface circuit and the MN/D output ports of the interface circuit corresponding to a pre-determined interstage exchange.

17. The switch as recited in claim 16 wherein the N/D first switching elements are arranged as a first stack of N/D parallel planes and the M/D second switching elements are arranged as a second stack of M/D parallel planes orthogonal to the first stack of planes.

18. The switch as recited in claim 15 wherein the interface circuit includes the first one, or the second one, or both the first one and the second one of the following circuitries:

(a) N/D first circuitries, each having M input ports to interconnect with the M output ports of one of the N/D first switching elements, and M output ports grouped into M/D output groups where each output group has D output ports,

(b) M/D second circuitries, each having N output ports to interconnect with the N input ports of one of the M/D second switching elements, and N input ports grouped into N/D input groups where each input group has D input ports, and

wherein the interface circuit further connects each output group of each one of the first circuitries to a distinct input group of a distinct one of the second circuitries.

19. The switch as recited in claim 18 wherein each one of the N/D first circuitries corresponds to an output exchange of one of the N/D first switching elements, and each of

the M/D second circuitries corresponds to an input exchange of one of the M/D second switching elements.

20. The switching network as recited in claim 15 wherein $M = P = 2^{n-r}$, $N = Q = 2^r$, and $D = 2^d$, with $1<r<n$ and $1\leq d<\min(r, n-r)$.

21. A switch comprising

N/D first switching elements arranged as a first stack of N/D parallel planes, each having P input ports and M output ports,

M/D second switching elements arranged as a second stack of M/D parallel planes orthogonal to the first stack of planes, each having N input ports and Q output ports, where $D > 1$, and D is a common factor of M and N,

a plurality of first adaptors, wherein every D output ports of each one of the N/D first switching elements are adapted by a first adaptor into a single bundle of output ports such that each one of the first switching elements has M/D bundles of output ports, and

a plurality of second adaptors, wherein every D input ports of each one of the M/D second switching elements are adapted by a second adaptor into a single bundle of

input ports such that each one of the second switching elements has N/D bundles of input ports, and wherein each one of the first switching elements is connected to each one of the second switching elements by the connection of a distinct one of the M/D bundles of output ports and a distinct one of the N/D bundles of input ports.

22. A method for routing a packet through a $2^{n-d}\times2^{n-d}$ k-stage bit-permuting network constructed from modified 2-stage interconnection, the packet having a destination address expressed as $D_1D_2...D_{n-d}$, the network including 2^{r-d} $2^{n-r}\times2^{n-r}$ input nodes, 2^{n-r-d} $2^r\times2^r$ output nodes, and an interstage exchange induced by a permutation π on integers from 1 to n−d such that the images of the numbers r−d+1, r−d+2, ..., n−d cover the numbers 1, 2, ..., n−r−d, or equivalently, the images of the numbers 1, 2, ..., r−d are covered by the numbers n−r−d+1, n−r−d+2, ..., n−d, for $1<r<n$ and $1\leq d<\min(r, n-r)$, $k>n-d$, the method comprising

generating a routing tag for the packet from the destination address $D_1D_2...D_{n-d}$ and the guide of the network expressed as $\gamma(1), \gamma(2), ..., \gamma(k)$, the routing tag being a k-symbol string $D_{\gamma(1)}D_{\gamma(2)}...D_{\gamma(k)}$, and

routing the packet at the j-th stage using $D_{\gamma(j)}$ in the routing tag.

23. The method as recited in claim 22 wherein, whenever the p-th symbol of the routing tag is equal to the q-th symbol, where p<q, disabling the whole stage of switching nodes at either stage-p or stage-q.